Dual-Gate MESFET Variable-Gain Constant-Output Power Amplifier

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Abstract—**The use of a dual-gate GaAs FET as a broad-band variable-gain and constant output power amplifier is described. A five-stage variable gain-constant output power amplifier has been realized which provides a constant output power of 3 dBm (±2 dB) for a large dynamic range of input power of −45 dBm to 0 dBm over the 4–8-GHz band. The amplifier uses a feed-forward AGC circuit for preadjusting the gain of the amplifier stages depending upon the strength of the signal at the output of preceding stages. The amplifier has the capability of detecting two or more simultaneous RF pulses having different amplitudes and separated by more than 15-ns time intervals. Also it preserves any amplitude modulation of the individual pulse.**

I. Introduction

IN THE PAST few years, the dual-gate FET has attracted considerable attention because of its being promising as a microwave multifunction device with a dual-gate structure. It can be used as a highly efficient switch or as a voltage programmable gain block that is rapidly integrated with GaAs FET TTL control logic. Dual-gate FET's have been used as mixers [1], multipliers [2], up-converters [3], discriminators [4], limiters [5], etc. Dual-gate FET's have the capability of providing high gain and high-speed modulation [6].

Since the first description of the dual-gate GaAs FET in 1971 [7], several papers, particularly on the subject of microwave variable gain amplifiers, have been published [8]–[10]. The gain of a dual-gate GaAs FET can be easily varied by varying the second gate bias voltage. This property of dual-gate FET amplifiers being capable of providing variable gain is utilized to provide a constant output power through a feed-forward automatic gain control circuit. In the AGC loop, the input signal of the amplifier is sampled, detected, and processed at video frequencies and applied to the second gate of the dual-gate FET amplifier to preadjust the gain of the amplifier depending upon the input signal strength. This paper presents a design and performance of a five-stage variable-gain constant output power amplifier. The amplifier to be described has the following key features. 1) It delivers constant output power of 3±2 dBm for any input power level from −45 dBm to 0 dBm. 2) It is a variable-gain linear amplifier meaning that none of the stages run into saturation for the entire dynamic range of the input power. The gain of the amplifier is electronically controlled to track the input power level to keep output power constant. 3) It preserves the amplitude modulation. 4) It has a response time of 15 ns. 5) It can detect two RF pulses separated by 15 ns of different amplitude (within its dynamic range) and delivers the output of the same amplitude (3±2 dBm). 6) The output RF power level of the amplifier is settable by an externally-supplied dc input voltage to the second gate of the final stage.

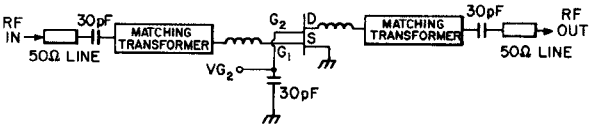

Fig. 1. Matching networks for a dual-gate FET amplifier.

The variable-gain constant-output power amplifier has a large number of system applications which require an input amplifier with the capability to handle a large dynamic signal range with variable gain and constant RF power output with extremely fast response. This amplifier finds application in long-range radars which are subjected to a wide variation in received echo signals. The amplifier lends itself to automated STC (sensitivity time control) while guarding against large amplitude signals that might overload the receiver. In electronic surveillance measures (ESM), the amplitude modulation of the radar pulse must be preserved by the countermeasure receiver. The conventional power limiter [5] does not have this capability. The variable-gain constant-output power amplifier will preserve the video amplitude coding of the radar pulse. This amplitude preservation is assured because the automatic gain adjustment will prevent saturation of the amplifier and amplitude clipping.

II. Single-Stage Dual-Gate FET Amplifier

A single-stage dual-gate FET amplifier is designed using an NEC 46300 dual-gate FET. The *S*-parameters of the FET are measured and then the input and output impedance matching circuits are designed using the CAD technique. These matching circuits are designed for realizing maximum gain from the first gate to drain of the dual-gate FET for a given gate and drain bias voltage with the second gate RF grounded. The circuit design used the COSMIC (computer optimization of Microwave Integrated Circuits) program developed at RCA Laboratories for opti-

Manuscript received September 2, 1980; revised October 28, 1980. This work was supported by the Naval Research Laboratory, Washington, DC, under the Contract N000173-78-C-0227, under the sponsorship of the Naval Electronics Systems Command.

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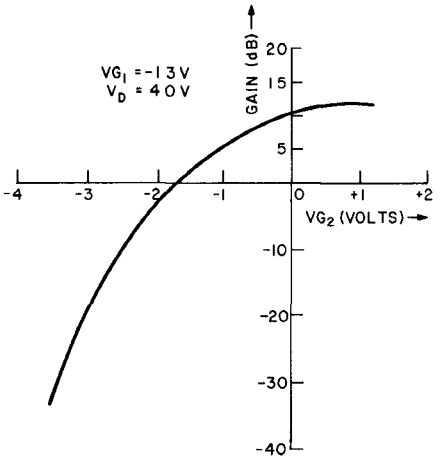


Fig. 2. Variation of gain of a dual-gate FET amplifier with second-gate bias. Frequency = 6 GHz.

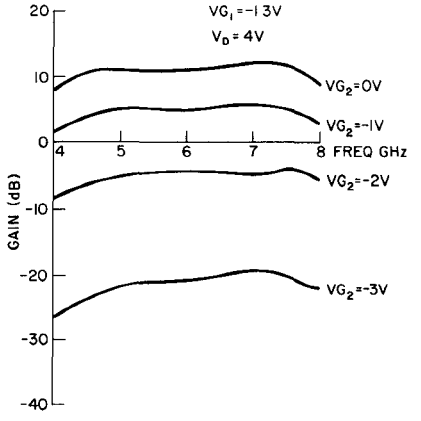


Fig. 3. Gain as a function of V_{G2} of dual-gate FET amplifier over 4–8-GHz band.

mizing the network design. Fig. 1 shows the block diagram of the single-stage dual-gate FET amplifier circuit. The variation of gain with the second-gate bias voltage is shown in Fig. 2. The variation of gain with frequency for different second-gate bias voltage is shown in Fig. 3. The single-stage amplifier has a gain of 10 dB minimum over 4.5–7.5 GHz. A single-stage dual-gate FET amplifier has a dynamic gain range of +10 to −30-dB gain for a second-gate control voltage variation of 0 to −3.5 V.

III. Linear Amplifier and AGC

The design of the linear amplifier with variable gain and constant output power is shown in Fig. 4. It is a five-stage amplifier. The first and last stages of the amplifier do not have built-in AGC. The first stage is intended for providing preamplification prior to sampling of an RF input signal and the last stage is intended for external setting of the output power. The external control input is applied at the second gate of the dual-gate FET in the last stage. The middle three stages are advanced AGC stages. The principle of the AGC unit is illustrated in Fig. 5. As shown in Fig. 5, the signal at the input of the amplifier is sampled through a 10-dB coupler and is detected and processed at video frequencies to dynamically preadjust the gain of the amplifier. The video output of the video amplifier is applied to the second gate of the dual-gate FET. The signal appearing at the second gate depends upon the input signal strength. Thus, the gain of the dual-gate FET amplifier is preadjusted in accordance with the input signal strength. The relationship between the gain of the video amplifier, sensitivity of the crystal detector, and the required variation of the gain of the dual-gate FET amplifier is determined, depending upon the input signal strength and required output power. From this relationship, the gain of the video amplifier is calculated. To obtain a constant output power from a single advanced AGC control unit, one requires the video amplifier gain to vary in accordance with the input signal. This could be achieved through having three AGC units. One requires more than one AGC unit for getting 45-dB dynamic range. As shown in Fig. 4, five stages are necessary to achieve the overall gain of 50 dB when the signal is at its lowest level.

It is determined that the video amplifier in the AGC control unit should have a gain of 40 dB and a bandwidth of greater than 350 MHz to provide enough control voltage to the second gate of the FET for dynamically controlling

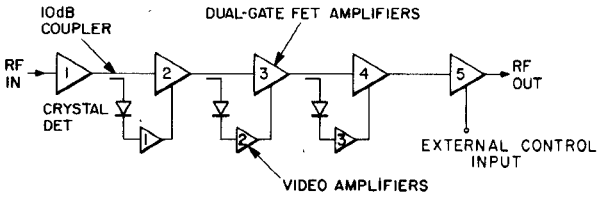


Fig. 4. Schematic of variable-gain constant-output power amplifier.

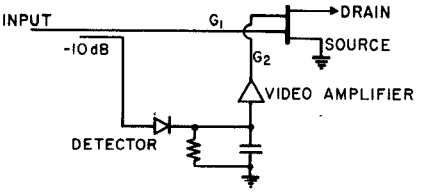


Fig. 5. Advanced AGC control.

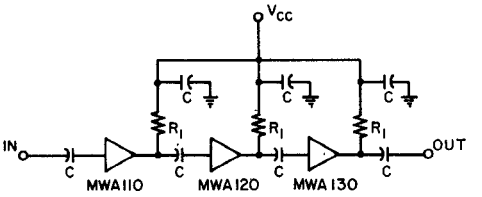


Fig. 6. Schematic of video amplifier.

TABLE I
CHARACTERISTICS OF VIDEO HYBRID AMPLIFIERS

rf HYBRID	FREQUENCY RANGE (MHz)	GAIN (dB)	NOISE FIGURE (dB)	OUTPUT at 1 dB COMPRESSION (dBm)
MHA 110	0.25-400	14	4	-2.5
MHA 120	0.25-400	14	5.5	+8.2
MHA 130	0.25-400	14	7.0	+18

THE CHARACTERISTICS OF THE THREE-STAGE VIDEO AMPLIFIER ARE

BANDWIDTH	0.25 TO 400 MHz
GAIN	40 dB
VOLTAGE OUTPUT (max)	2.5 V
LOAD IMPEDANCE	50 OHMS

the gain and for meeting the fast response time. A three-stage video amplifier is designed using Motorola RF hybrids MWA 110, MWA 120, and MWA 130 in cascade. The schematic of the amplifier is depicted in Fig. 6, and the characteristics of each RF hybrid amplifier are given in Table I.

IV. Performance and Results

The photograph of the five-stage AGC amplifier is shown in Fig. 7. The variation of output power of the amplifier as a function of frequency for different input power levels (−45 dBm to 0 dBm) is shown in Fig. 8. The variation of output power is within ±2 dB in the 4.5 to 7.5-GHz frequency range of a variation in input power levels of −45 dBm to 0 dBm. The pulse response of the amplifier is tested for two different simultaneous input pulses of different amplitudes separated by 15 ns. Fig. 9(a) shows the two input RF pulses of different power levels separated by 15 ns. The pulse width is 300 ns for both pulses. Fig. 9(b) shows the output RF pulses corresponding to the input pulses shown in Fig. 9(a). It is seen from Fig. 9(b) that the output pulses are of the same amplitude and the amplitude of each is within the range (3±2 dBm). Fig. 10(a) and 10(b) show the amplitude modulated input and output

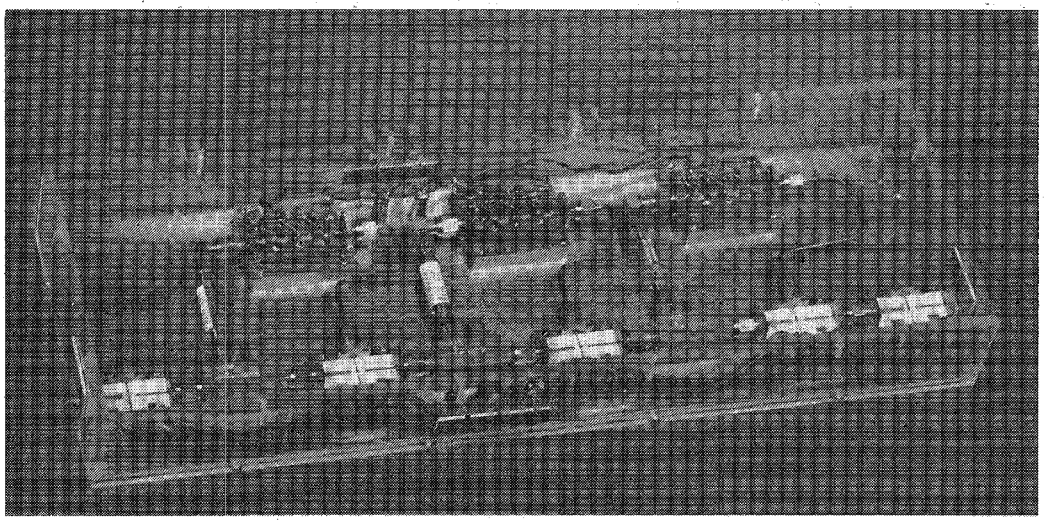


Fig. 7. Photograph of the amplifier.

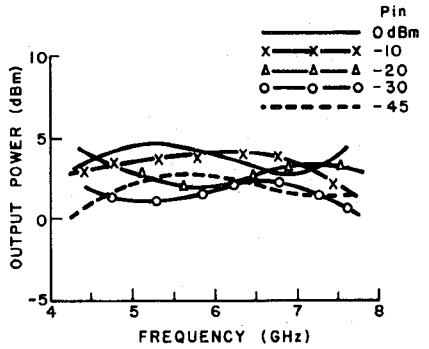
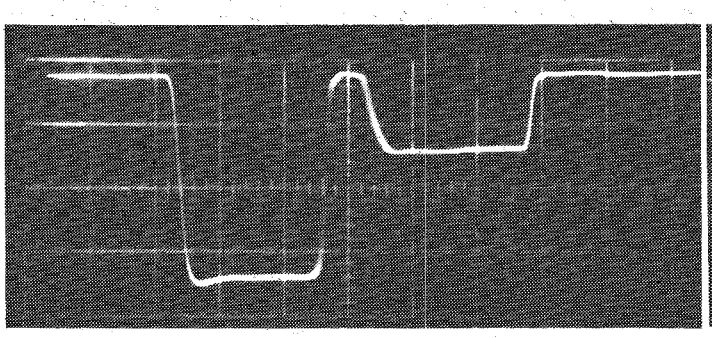
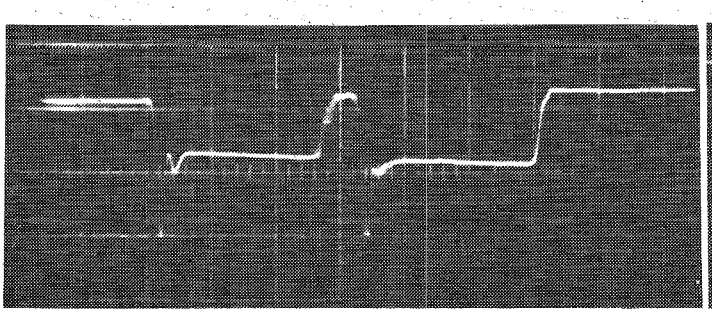


Fig. 8. Variation of output power with frequency for different input power levels.

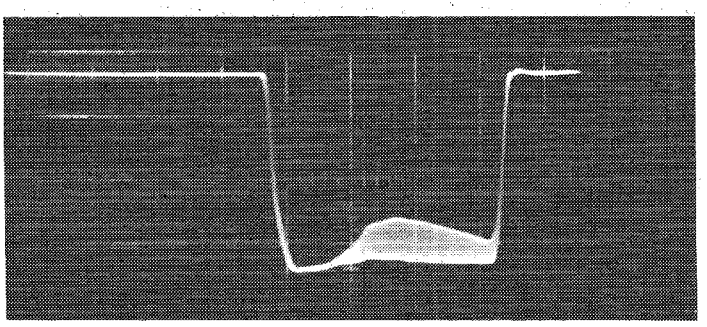


(a)

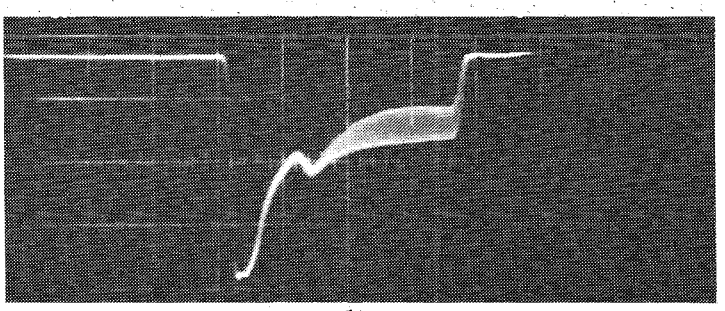


(b)

Fig. 9. (a) Two input RF pulses of different amplitudes. Scale: horizontal: 100 ns/div; vertical: 0.02 V/div. (b) RF output pulses. Scale: horizontal: 100 ns/div; vertical: 0.1 V/div.



(a)



(b)

Fig. 10. (a) Amplitude modulated input RF pulse. Scale: horizontal: 100 ns/div; vertical: 0.1 V/div. (b) Amplitude modulated output RF pulse. Scale: horizontal: 100 ns/div; vertical: 0.1 V/div.

pulses. The input pulse is modulated with a 3-MHz sinusoidal signal. The amplifier successfully retains the modulation envelope.

V. Conclusions

A variable-gain constant output power amplifier has been presented. The variable gain is obtained with a dual-gate FET amplifier and the constant output power is obtained through advanced AGC. The automatic gain adjustment prevents saturation of the amplifier and amplitude clipping. The amplifier has a wide dynamic range of the input signal of −45 dBm–0 dBm over a 3-GHz band. The amplifier described above has many applications as cited in Section I which makes it very versatile for multifunctional use. The amplifier has the capability of detecting two (or more) pulses at a fast rate and of preserving the amplitude modulation and has a wide bandwidth and dynamic range as well.

Acknowledgment

The authors are grateful to H. J. Wolkstein and R. E. Askew for their encouragement and helpful discussions, to D. W. Bechtle and S. A. Siegel for the design and fabrication of the video amplifier, and to E. Mykietyn, P. A. Czajkowski, and R. J. Menna for their skillful fabrication of the amplifier.

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Synthesis of Broad-Band 3-dB Hybrids Based on the 2-Way Power Divider

G. LENNART NYSTRÖM

Abstract— **The synthesis of broad-band 2-way Wilkinson hybrids is well known. The even- and odd-mode analysis results in two equivalent circuits where the synthesis of the odd mode is done by computer optimization. This paper shows an exact synthesis of 2-way Wilkinson power dividers having one isolation resistor, but an arbitrary number of quarter-wave transformers. A large number of circuits have been synthesized with up to 6 quarter-wave transformers. The 2-way Wilkinson hybrid can be extended to a 4-port component. This 4-port component can operate as a 180° or 90° 3-dB hybrid depending on the input port. The hybrid has a high directivity independent of frequency when used as a 180° hybrid. Experimental results are given for a 2-way divider and a 3-dB hybrid built in microstrip with a center frequency of 5 GHz.**

I. Introduction and Theory

BROAD-BAND 2-way Wilkinson power dividers (Fig. 1) are synthesized by using the even and odd modes [1]–[4]. The synthesis of the even mode is exact and well known. The synthesis of the odd mode has previously been carried out only by computer optimization. This paper shows how to make an exact synthesis of the odd mode when only one isolation resistor is employed (Fig. 2). The problem is that of an *n*-order matching with the character-

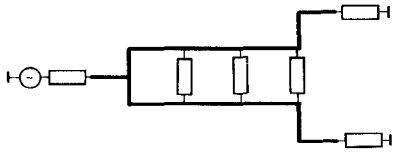

Fig. 1. The 2-way Wilkinson power divider.

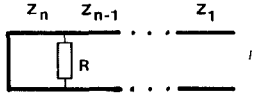

Fig. 2. The new odd-mode circuit.

Manuscript received July 23, 1980; revised October 27, 1980.
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